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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,872	08/01/2003	Joseph H. End III	TN302	4647

7590 07/09/2007

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EXAMINER	
CHERY, MARDOCHEE	
ART UNIT	PAPER NUMBER
2188	
MAIL DATE	DELIVERY MODE
07/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/632,872	END, JOSEPH H.	
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-12,14-18,21-22* is/are rejected.

7)☒ Claim(s) *7,13,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to Applicant's communication filed on April 5, 2007 in response to PTO Office Action mailed on January 25, 2007. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the Office Action mailed on January 25, 2007, claims 1, 9, 15, 17, and 21 are amended. Claims 1-22 remain pending.

Response to Arguments

3. Applicants' representatives argue on page 11, paragraph 3 of the remarks that "it would have not been obvious to combine the synchronizer of Shiozaki with the multimode memory system of Nystuen.

Examiner respectfully disagrees. Nystuen's relates to "a memory controller including a request input for receiving successive memory access requests and a memory controller for use with memory devices having multiple banks (Abstract; par. 0001)" and Shiozaki's relates to "a storage control system that controls the update operations on two buffer address arrays in a data processing system (Abstract). For a synchronizer merely ensures that devices at the transmitting and receiving end, multiple devices or agents, performing specific time critical tasks operate together in a fixed phase relationship, one of ordinary skill in the art

would have recognized that the synchronizer of Shiozaki could be implemented in any system performing data requests having multiple memory devices or multiple memory banks such as in Nystuen's.

4. Applicants' representatives' arguments with respect to claims 1 and 17, filed April 5, 2007 have been considered but are moot in view of the new ground(s) of rejection over Payson (7,193,994).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-6, 8-12, 14-18, 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nystuen (2004/0088472) in view of Shiozaki et al. (4,683,533) and further in view of Payson (7,193,994).

As per claim 1, Nystuen discloses a memory controller for managing memory requests from a plurality of requesters to a plurality of memory banks, the memory controller comprising: an arbiter configured to receive the memory requests from the

plurality of requesters, the arbiter assigning a first memory request to a first processing path and a second memory request to a second processing path responsive to the memory banks requested by the received and assigned memory requests [Fig. 3; par. 3]; a first path controller coupled to the arbiter and the plurality of memory banks, the first path controller configured to process the first memory request in the first processing path to activate a first memory bank associated with the first memory request for a first data transfer [Figs. 3 and 5; pars. 28-30]; a second path controller coupled to the arbiter and the plurality of memory banks, the second path controller configured to process the second memory request in the second processing path to activate, during the first data transfer, a second memory bank associated with the second memory request for a second data transfer [Figs. 1 and 3; pars. 23-28].

However Nystuen does not explicitly teach a second path controller configured to process the second memory request in the second processing path as required by the claim.

Shiozaki discloses a second path controller configured to process the second memory request in the second processing path [col.4, lines 27-29; col.1, lines 8-15; col.3, lines 31-36; col.1, lines 25-27; col.2, lines 39-42] and a synchronizer coupled between the first path controller and the second path controller for synchronizing the first and second path controllers such that the first and second memory requests processed by the first and second path controllers, respectively, do not conflict [col. 1, ll

33-38; col. 2, ll 17-23 and col. 3, ll 25-36] to prevent a conflict from taking place during an update operation (col. 2, ll 17-23).

Since the technology for implementing a memory controller with a second path controller configured to process the second memory request in the second processing path was well known as evidenced by Shiozaki, an artisan would have been motivated to implement this feature in the system of Nystuen in order to avoid conflict during an update operation. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Nystuen to include a second path controller configured to process the second memory request in the second processing path because this would have prevented conflict from taking place during an update operation (col. 2, ll 17-23) as taught by Shiozaki.

However, Nystuen and Shiozaki do not explicitly teach an arbiter having a plurality of request ports, each request port configured to receive the memory requests from a respective one of the plurality of requesters, and the first and second data transfers do not conflict.

Payson discloses an arbiter having a plurality of request ports, each request port configured to receive the memory requests from a respective one of the plurality of requesters [col. 9, ll 40-60, and a synchronizer synchronizing first and second path controllers such that the first and second data transfers do not conflict [col. 9, ll 47-63; col. 11, ll 1-20] to control a plurality of devices configured to transmit and receive data at

high speed and keep them in synchronization and resolve any conflicts that may arise (col. 4, ll 9-23; col. 9, ll 50-60).

Since the technology for implementing a memory controller with an arbiter having a plurality of request ports, each request port configured to receive the memory requests from a respective one of the plurality of requesters, and the first and second data transfers do not conflict was well known as evidenced by Payson, an artisan would have been motivated to implement this feature in the system of Nystuen and Shiozaki in order to control a plurality of devices configured to transmit and receive data at high speed and keep them in synchronization and resolve any conflicts that may arise. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Nystuen and Shiozaki to include an arbiter having a plurality of request ports, each request port configured to receive the memory requests from a respective one of the plurality of requesters, and the first and second data transfers do not conflict because this would helped with controlling a plurality of devices configured to transmit and receive data at high speed and keep them in synchronization and resolve any conflicts that may arise (col. 4, ll 9-23; col. 9, ll 50-60) as taught by Payson.

As per claim 2, Shiozaki discloses the arbiter, the first path controller, the second path controller, and the synchronizer are implemented as a single field programmable gate array [col.4, lines 27-29; col.1, lines 8-15; col.3, lines 31-36; col.1, lines 25-27].

As per claim 3, Nystuen discloses the arbiter, the first path controller, the second path controller, and the synchronizer are configured for use with an SDRAM memory device comprising the first and second memory banks [Figs. 3 and 5].

As per claim 4, Nystuen discloses a first path timing controller that controls the first path circuitry and activates the first memory bank associated with the first memory request [Figs. 8-9]; and address and data multiplexers that multiplex addresses and data associated with the first memory request for interfacing with the memory banks [Fig. 5; MUX 520]; a second path timing controller that controls the second path circuitry and activates the second memory bank associated with the second memory request [Figs. 8-9]; and the address and data multiplexers that multiplex addresses and data associated with the first memory request, the address and data multiplexers further multiplexing addresses and data associated with the second memory request for interfacing with the memory banks [Fig. 5; MUX 520].

However, Nystuen does not explicitly teach the first path controller comprises at least: first path circuitry that passes addresses and data associated with the first memory request; and wherein the second path controller comprises at least: second path circuitry that passes addresses and data associated with the second memory request as required by the claim.

Shiozaki discloses the first path controller comprises at least: first path circuitry that passes addresses and data associated with the first memory request [Fig. 1; col. 2,

ll 1-5 and ll 12-28]; and wherein the second path controller comprises at least: second path circuitry that passes addresses and data associated with the second memory request [Fig. 1; col. 1, ll 6-15 and ll 51-60] to prevent a conflict from taking place during an update operation (col. 2, ll 17-23).

Since the technology for implementing a memory controller with a first path circuitry that passes addresses and data associated with the first memory request and a second path circuitry that passes addresses and data associated with the second memory request was well known as evidenced by Shiozaki, an artisan would have been motivated to implement this feature in the system of Nystuen in order to avoid conflict during an update operation. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Nystuen to include a first path circuitry that passes addresses and data associated with the first memory request and a second path circuitry that passes addresses and data associated with the second memory request because this would have prevented conflict from taking place during an update operation (col. 2, ll 17-23) as taught by Shiozaki.

As per claim 5, Shiozaki discloses the synchronizer comprises: delay circuits coupled between the first and second path controllers to set delay values therebetween to adjust the timing of the first and second path controllers during processing of the first and second memory requests responsive to the first and second memory requests [col. 2, ll 48-57 and col. 3, ll 18-24].

As per claim 6, Nystuen discloses the first path controller is further configured to initialize and refresh the plurality of memory banks [par. 73].

As per claim 8, Nystuen discloses the arbiter assigns the second memory request to the second path controller when the first path controller is active if the first and second memory banks are not equal [Fig. 3].

As per claim 9, the rationale in the rejection of claim 1 is herein incorporated.

As per claim 10, the rationale in the rejection of claim 4 is herein incorporated.

As per claim 11, the rationale in the rejection of claim 5 is herein incorporated.

As per claim 12, Nystuen discloses initializing the plurality of memory banks using the first processing path [par. 50].

As per claim 13, Nystuen discloses receiving the memory requests from the plurality of memory requesters during a current arbitration cycle [par. 30]; comparing the plurality of memory requesters to a grant history register identifying the plurality of memory requesters that have had previous memory requests granted during the current cycle [pars. 45- 47]; identifying the first memory request by a first memory requester

from the plurality of memory requesters not on the grant history register and not having a current request in the second processing path using fixed priority logic [pars. 30 and 34]; and adding the first memory requester to the grant history register [par. 32].

As per claim 14 the rationale in the rejection of claim 8 is herein incorporated.

As per claim 15 the rationale in the rejection of claim 9 is herein incorporated.

As per claim 16, Nystuen discloses means for combining the first and second memory requests for accessing the plurality of memory banks, wherein the processing means comprises generating a read command or a write command in each of the first and second processing paths and wherein the commands are concatenated by synchronizing and combining means [Fig. 3; pars. 28 and 32].

As per claim 17, the rationale in the rejection of claim 13 is herein incorporated. Payson further discloses assigning a memory request to one of the at least one controllers from one of the identified plurality of memory requesters that have not had previous memory requests granted during the current arbitration cycle using fixed priority logic [col. 7, ll 44-52; col. 12, ll 57 to col. 13, ll 3; col. 13, ll 49-55] in order for the arbiter to grant a source device a time slot to transmit data to a destination device (col 12, ll 50-56).

As per claim 18, Nystuen discloses identifying from the plurality of memory requesters not on the grant register a lowest memory requester having a lowest value among the plurality of memory requesters not on the grant history register for assignment to one of the at least one controller [pars. 45-47].

As per claim 21, the rationale in the rejection of claim 13 is herein incorporated.

As per claim 22, Nystuen discloses the arbiter and the at least one path controller are implemented in a field programmable gate array [par. 31].

Allowable Subject Matter

7. Claims 7, 13, 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

10. When responding to the Office action, Applicant is advised to clearly point out where support, with reference to page, line numbers, and figures, is found for any amendment made to the claims.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

July 3, 2007

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
7/05/07

Mardochee Chery
Examiner
AU: 2188